



Built-In Self-Test for Input/Output Buffers

By Sudheer Vemula

Book Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | FPGAs & SOCs | Programmable Input/Output (I/O) cells are an integral part of any Field Programmable Gate Array (FPGA). The resources associated with the programmable I/O cells are increasing as newer architectures of FPGAs are being developed and this increases the importance of testing them. A general Built-In Self-Test (BIST) architecture to test the programmable I/O cells in FPGAs or associated with the FPGA core of System-on-Chip (SoC) implementations is proposed. The I/O cells are tested for various modes of operation along with their associated programmable routing resources. The proposed BIST architecture has been implemented and verified on Atmel AT94K10 and AT94K40 SoCs. A total of 161 and 303 configuration downloads are required to test the I/O cells of AT94K10 and AT94K40 devices, respectively. The use of an embedded processor for dynamic partial reconfiguration reduced the number of configuration downloads to three for both the AT94K10 and AT94K40 devices. The implementation of dynamic partial reconfiguration gave a speed up of 99.39 times in test time and a reduction in configuration memory storage requirements by 101 times for AT94K40 devices. | Format: Paperback | Language/Sprache: english | 100 pp.

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